2819

Attorney Docket No.: YOR9-2001-0512 (728-218)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: Joshi et al.

EXAMINER: Cho, James Hyongchol

COPY OF PAPERS ORIGINALLY FILED

SERIAL NO.: 09/900,302

GROUP ART UNIT: 2819

FILED: July 6, 2001

DATED: July 1, 2002

FOR: LOGIC OR CIRCUIT

Assistant Commissioner for Patents
Washington, DC 20231

AMENDMENT TRANSMITTAL FORM

Sir:

Transmitted herewith is an amendment in the above-identified application.

[ ] Small entity status of this application under 37 C.F.R. §§1.9 and 1.27 has been established by a verified statement previously submitted.

[ ] A verified statement to establish small entity under 37 C.F.R. §§1.9 and 1.27 is enclosed.

[X] No additional fee is required.

For	Claims Remaining After Amendment	Highest No. Previously Paid For	Present Extra	Rate (Small Entity)	Addit. Fee	Rate	Addit. Fee
TOTAL CLAIMS*	8	20	0	x 9 =	$0	x 18 =	$0
INDEPENDENT CLAIMS	1	3	0	x 40 =	$0	x 80 =	$0
[] First Presentation of Multiple Dep. Claim				135		270	$0

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

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Dated: July 1, 2002

Bridget Griffin

[ ] Please charge Deposit Account No. 04-1121 in the amount of $___. Two (2) copies of this sheet are enclosed.

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[X] Please charge any deficiency as well as any other fee(s) which may become due under 37 C.F.R. §§1.16 and/or 1.17 at any time during the pendency of this application, or credit any overpayment of such fee(s) to Deposit Account No. 04-1121. TWO (2) COPIES OF THIS SHEET ARE ENCLOSED.

Respectfully submitted,

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Washington, DC 20231

REPLY

Sir:

In response to the Office Action dated March 29, 2002, please amend the Application as set forth below.

IN THE CLAIMS:

Please amend Claims 1-2, 4-9 as follows and cancel Claim 3 without prejudice.

1. (Once Amended) A MOSFET logic circuit for performing a logic OR operation comprising three transistors, first and second transistors of the three transistors forming a transmission gate outputting one signal, and wherein at least two input signals are provided to the first and second transistors and an output signal indicative of an OR operation performed on a first and second input signal of the at least two input signals is output from the MOSFET logic circuit.

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Dated: July 1, 2002

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